CASE STUDY

FPGA-Based Control & Interface Electronics for a Tunable NIR Spectrometer

Optics for Hire.

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Prepared for:

A near-infrared spectroscopy instrument company

Project Type:

Multi-phase electronics design — FPGA firmware, custom SMD PCB design, USB 2.0 interface, CCD interface board analysis & debug

Project Years:

2008-2013

1. Executive Summary

Optics for Hire (OFH) provided multi-phase electronics engineering services to a near-infrared spectroscopy instrument company over a five-year engagement. The work spanned FPGA firmware development and board bring-up support for an early spectrometer platform, a full custom PCB design for a scanning-mirror tunable device controller, and detailed interface board analysis and debug for a CCD-based spectrometer. Across these phases, OFH delivered FPGA/NIOS firmware, custom SMD PCB designs with full BOM, USB 2.0 high-speed interface implementation, analog front-end design for PbS and InGaAs photodetectors, and systematic diagnosis and remediation of USB, CCD voltage, CCD clock timing, and analog signal integrity issues.

KEY RESULT	Multi-phase electronics program: FPGA/NIOS firmware for spectrometer control, custom FPGA + USB 2.0 HS + 16-bit ADC PCB design for scanning-mirror tunable NIR device, and full interface board debug covering USB signal integrity, CCD voltage/timing, and analog channel black-level correction — all delivered with Altium design files.

2. Background & Client Context

The client develops tunable near-infrared (NIR) spectrometers used in applications including chemical analysis, process monitoring, and medical diagnostics. NIR spectrometers based on tunable Fabry-Perot filters, scanning mirrors, or liquid crystal tunable elements require sophisticated control electronics to synchronize the tuning element with the detector readout — coordinating timing signals, digitizing photodetector output at high speed, and transferring data to a host PC at rates that demand USB 2.0 high-speed operation.

OFH was engaged across multiple instrument generations to provide electronics engineering support that the client's did not maintain in-house. The engagement covered three distinct phases, each addressing a different instrument variant or technology generation.

3. Phase 1: FPGA Firmware & Board Bring-Up (2008)

3.1 Scope

The first engagement involved FPGA firmware support and board bring-up assistance for an existing spectrometer platform. The client's team encountered issues during production programming of the Altera EPCS4 serial configuration device — a non-volatile memory that stores both the FPGA configuration bitstream and the embedded NIOS II soft-processor firmware. Boards that had been operating correctly were failing after reprogramming.

3.2 Technical Issues Resolved

- EPCS4 reprogramming procedure: clarified that the JIC (JTAG Indirect Configuration) file format combines both the FPGA configuration and NIOS firmware into a single programming file. Reprogramming the EPCS4 with to restore both.
- Board version compatibility: identified that a connector pinout mirror change between the first and subsequent board revisions meant the JIC file compiled for the first board was not compatible with the remaining four boards — a separate firmware build was required for the mirrored connector layout.
- Documented the standard download procedure for both FPGA and NIOS in a single programming step.

4. Phase 2: Scanning Mirror Tunable Device Controller

4.1 Project Scope

The second engagement was a full custom electronics design — a new control and interface board to adapt the client's existing tunable Fabry-Perot spectrometer platform to a resonant scanning mirror tunable element. The scanning mirror approach required different timing and control electronics compared to the original tunable filter design: the mirror position must be tracked in real time from the driver phase signals, synchronized precisely with the detector integration window, and the digitized spectral data transferred to the host PC at up to 1000 spectral points per 1.3 ms — a data rate requiring USB 2.0 high-speed operation.

DESIGN CHALLENGE	A resonant scanner operates at a fixed mechanical resonant frequency (up to 5 kHz), with the instantaneous mirror position encoded in the phase of the drive signal. Capturing a full NIR spectrum requires acquiring up to 1000 photodetector samples during a single half-period of the mirror sweep (1.3 ms), demanding ADC conversion rates and FPGA data buffering far beyond what the prior Fabry-Perot platform required.

4.2 System Architecture

The board was designed around an Altera Cyclone III FPGA (EP3C10) as the central control element, coordinating all timing signals, managing data flow between the ADC, detector interface, and USB subsystem, and implementing the communication protocol. Key architectural decisions made during the design phase:

- USB interface: upgraded to USB 2.0 high speed (480 Mbit/s) via the FTDI FT245R USB FIFO bridge, enabling the free-run acquisition bandwidth of approximately 8 MB/s required for 1000-point spectra at 5 kHz scan rate. RS-232 retained for command-only communication at auto-baud rate for instrument control in snapshot mode.
- ADC selection: 16-bit, 1.33 MSPS Analog Devices AD7983 (primary high-speed channel) and 16-bit 250 kSPS AD7685 (auxiliary channels for thermistor and slow signals). Signal quality was prioritized over

cost — ADCs were placed on the board location offering shortest signal path from detector, even where that placement added cost vs. a shared daughter-board approach.

- Detector interfaces: PbS detector (Hamamatsu P9217) and InGaAs PIN photodiode (Hamamatsu G5853) both supported, with switchable front-end gain stages using Analog Devices AD8615 rail-to-rail op-amps. Precision voltage references (ADR391/ADR392) maintain ADC accuracy across temperature.
- Resonant scanner interface: SC-3-5 scanner (7×7 mm and 12×7 mm versions) phase signals intercepted and digitally decoded in the FPGA to extract mirror position. All timing signals for scan synchronization generated by the FPGA.
- TEC temperature monitoring: two thermistors (TEC temperature and device body temperature) read via 16-bit ADC channels and stored digitally for instrument compensation.
- APD bias supply: Maxim MAX15031 80V boost converter provides adjustable APD bias voltage for avalanche photodiode detector variants.
- Power management: LT3471 dual boost/inverter for ±analog rails, LM3671 step-down converters for FPGA and digital 3.3V/1.2V rails, LP3874 LDO for precision analog 2.5V reference supply. Total power budget <500 mW.

4.3 Electrical Specifications

Parameter	Specification
Primary FPGA	Altera Cyclone III EP3C10, 144-pin EQFP, 50 MHz clock (Abracon ASE-50.000MHZ)
Configuration memory	Altera EPCS4, 4 Mbit serial flash (FPGA + NIOS firmware)
USB interface	FTDI FT245R USB/Parallel FIFO, USB 2.0 Full Speed (upgradeable to HS)
RS-232 interface	Maxim MAX3232E, auto baud rate, command protocol only
Primary ADC	Analog Devices AD7983, 16-bit, 1.33 MSPS PulSAR, MSOP/QFN
Auxiliary ADCs	Analog Devices AD7685, 16-bit, 250 kSPS (×2, for slow channels)
Voltage references	ADR391 (1.2V), ADR392 (2.5V), ADR130 (sub-bandgap) — Analog Devices
Op-amps (signal chain)	AD8615 CMOS rail-to-rail, 20 MHz, precision (×4)
Op-amps (biasing)	LF353 JFET dual (×6, for detector bias networks)
Detector inputs	PbS (Hamamatsu P9217), InGaAs PIN (Hamamatsu G5853)
Resonant scanner	EOPC SC-3-5, 7×7 mm and 12×7 mm, up to 5 kHz
Data acquisition speed	Up to 1000 points in 1.3 ms (1000-point option)
Integration time range	0.5 ms to 30 s, 0.5 ms steps

Parameter	Specification
APD bias supply	Maxim MAX15031, 80V boost, 300 mW
Board size	<60 × 96 mm (target)
Operating temperature	0°C to +70°C (circuits); −40°C to 0°C (TEC range)
Power consumption	<500 mW total
Material compliance	RoHS compliant throughout
Communication interfaces	USB 2.0 HS, RS-232, ADD/DAT Bus (DPRAM direct access)
Control signals	PWM (adjustable duty cycle), 8× GPIO, Trigger In, Trigger Out

4.5 Board Overview

The completed board was delivered as a compact SMD assembly targeting the <60×96 mm form factor. The design includes JTAG programming access for FPGA firmware updates, power connectors, USB and RS-232 interface ports, and the CCD connector for the detector daughter board. The 3D board render below shows the component placement density characteristic of a high-performance mixed-signal instrument board in this size class.

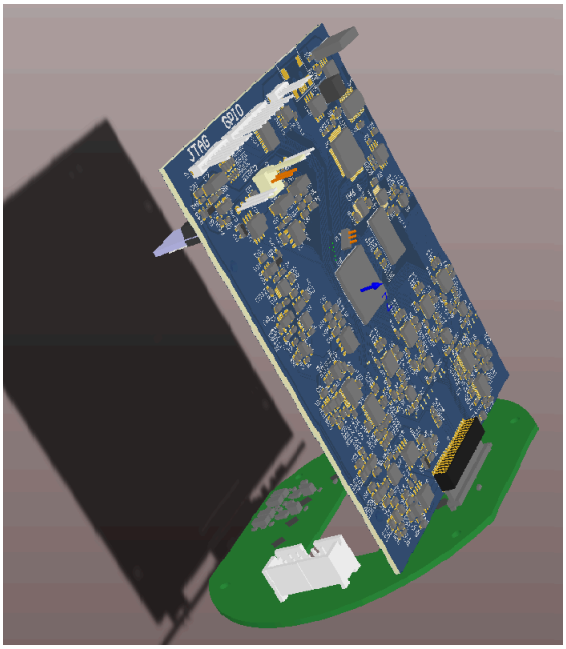


Figure 1: 3D rendered view of the custom spectrometer interface board. The Altera Cyclone III FPGA (large QFP at center), FTDI USB FIFO, ADC ICs, power management section, and CCD interface connector are visible. JTAG programming header at upper left. The compact layout accommodates the full analog, digital, and power management circuitry within the target form factor.

4.6 Deliverables

- 5 pieces of debugged, functioning prototype boards
- Complete BOM with US distributor part numbers (Digi-Key, Mouser, Newark)
- Schematics and PCB layout in Altium Designer (native format, not PDF)
- FPGA firmware source code (Quartus project, VHDL/Verilog)
- NIOS II embedded software source code and compiled binary (.hex)
- USB driver source code for FTDI FT245R
- Sample host PC program in C/C++
- Hardware and software user documentation
- Detailed system design description for BaySpec system integration

5. Phase 3: CCD Interface Board Analysis & Debug

5.1 Scope

In 2013, OFH was re-engaged to perform a systematic hardware and firmware analysis of the client's CCD-based spectrometer interface board. The board used a Perkin Elmer RL-series linear CCD array (RL1024PAG-021, RL1024PAQ-021, or RL2048PAQ-021) with an FTDI FT2232 dual-channel USB interface. The client was experiencing intermittent USB disconnections and unreliable CCD readout. OFH performed a structured diagnostic program covering the USB interface, CCD voltage levels, CCD clock timing, and the analog signal chain.

5.2 USB Interface Diagnosis

OFH developed a custom USB test program to isolate the FT2232 connectivity issues, enabling systematic characterization of USB device behavior under different cable and hub conditions. The diagnostic identified two root causes:

- Insufficient USB bus current: the USB port could not provide the current required by the FT2232 operating in high-speed mode. Oscilloscope measurement showed signal amplitude reduction on the FTDI clock output when using the failing cable. Resolution: specify use of a dual-power USB cable (drawing power from two USB ports) with an integrated ferrite filter.
- USB hub noise sensitivity: certain USB 2.0 hubs inject sufficient noise onto the USB lines to cause the FT2232 to hang. Resolution: add 47 pF capacitors to ground on both USB D+ and D− lines (reworked onto existing boards via soldering); specify USB 2.0 compliant cable (controlled wave impedance and shielding); update host software to detect non-responsive device and perform automatic reconnection via Windows API.

5.3 CCD Socket Mechanical Problem

Physical inspection of the board revealed that the CCD sensor socket had bent pins on the right side, preventing reliable seating of the sensor. The right side of the sensor could be inadvertently removed when the socket latch was closed. This was identified and documented before electrical measurements began, as a misseated sensor would have prevented any meaningful signal characterization.

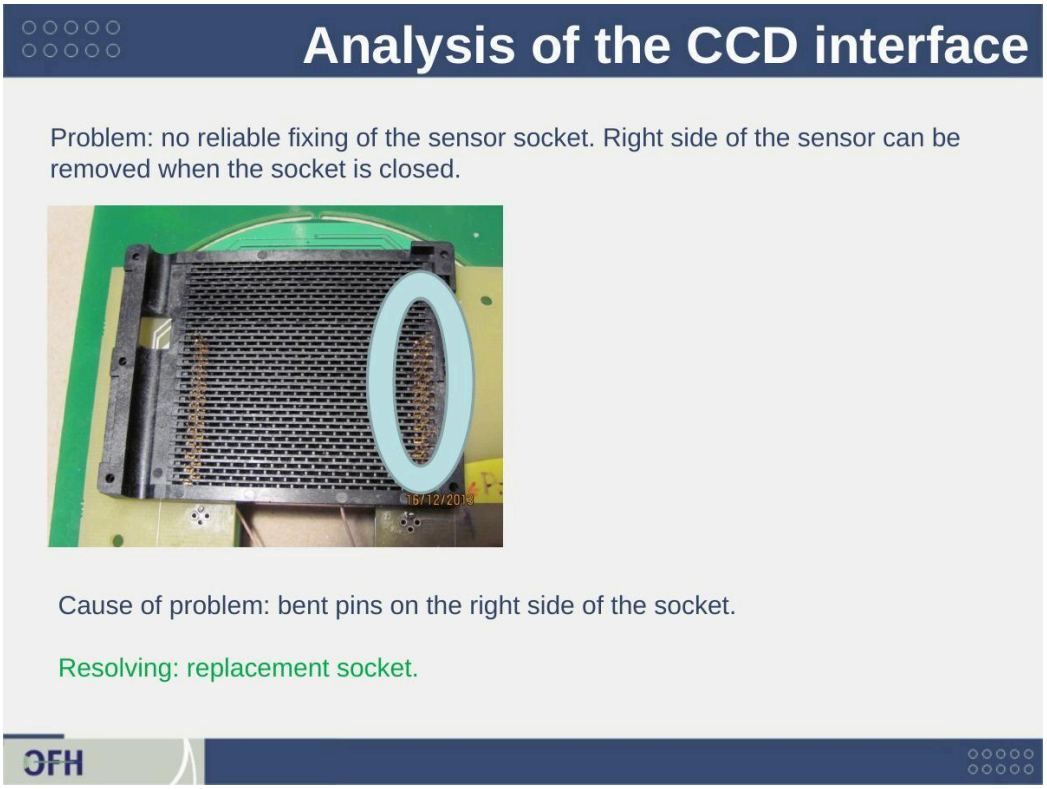


Figure 2: CCD sensor socket with bent pins (circled) on the right side preventing reliable retention of the Perkin Elmer RL-series CCD. Physical inspection identified this mechanical issue before electrical measurements began. Resolution: socket replacement.

5.4 CCD Voltage Level Analysis

OFH measured all CCD drive signal voltages with an oscilloscope and compared them against the Perkin Elmer CCD datasheet. The CCD pinout (46 pins) and DC operating characteristics were used as the reference specification. Multiple voltage levels were found out of specification across the vertical clock, supply, and horizontal clock domains.

Analysis of the DC characteristics

Description of tasks: verifying the signals on CCD with an oscilloscope, comparison the DC characteristics with the documentation.

PINOUT			
1	VSS	THERM1-	24
2	V1	THERM1+	25
3	V2	V1	26
4	V3	V2	27
5	OR-UR	V3	28
6	VRD-UR	VTG	29
7	VO-UR	OR-LR	30
8	VDD-UR	VRD-LR	31
9	HSG	VDD-LR	32
10	H3	VO-LR	33
11	H1	VOG	34
12	H2	H2	35
13	VOG	H1	36
14	VO-UL	H3	37
15	VDD-UL	HSG	38
16	VRD-UL	VDD-LL	39
17	OR-UL	VO-LL	40
18	VTG	VRD-LL	41
19	V3	OR-LL	42
20	V2	V3	43
21	V1	V2	44
22	THERM2+	V1	45
23	THERM2-	VSS	46

DC OPERATING CHARACTERISTICS

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
V_{DD}	DC Supply Voltage	18	24	28	V
V_{RD}	Reset Drain Voltage	13	14	18	V
V_{OG}	Output Gate Voltage	- 5	-2.5	1	V
V_{SS}	Substrate Ground	0	0	0	V

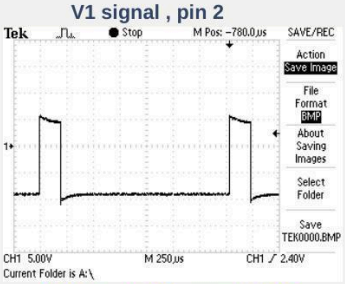
TYPICAL CLOCK VOLTAGES

SYMBOL	PARAMETER	HIGH	LOW	UNIT
ΦH_1, ΦH_2, ΦH_3	Horizontal Register Clocks	+5	-5	V
ΦSG	Summing Gate Clock	+9	-5	V
ΦV_1, ΦV_2	Vertical Register Clock	+2.5	-8.5	V
ΦV_3	Vertical Register Clock	+4.5	-6.5	V
ΦR	Reset Clock	+10	2	V
ΦVTG	Array Transfer Gate Clock	+4.5	-6	V

Figure 3: CCD pinout (46-pin, left) and DC operating characteristics / typical clock voltage tables from the Perkin Elmer RL-series datasheet, used as the measurement reference. Key specifications: ΦV1/ΦV2 vertical clocks HIGH = +2.5V, ΦV3 HIGH = +4.5V, horizontal clocks ΦH = +5V/−5V, VDD supply = 24V nominal.

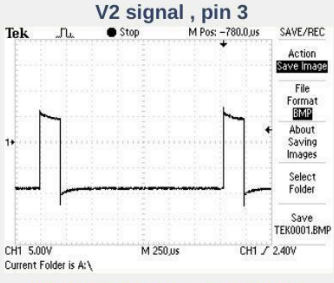
Analysis of the DC characteristics

V1 signal , pin 2



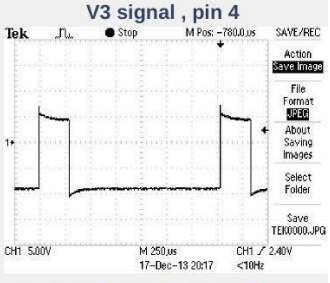
High level +5V , need +2.5V

V2 signal , pin 3



High level +5V , need +2.5V

V3 signal , pin 4



Low level -9V , need -6.5V

Resolving: check & correct the level formation scheme

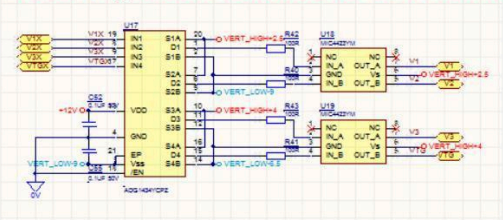


Figure 4: Oscilloscope measurements of V1 (pin 2), V2 (pin 3), and V3 (pin 4) vertical clock signals showing out-of-spec levels. V1 and V2 measured +5V high (required +2.5V); V3 measured −9V low (required −6.5V). The level formation schematic (bottom) identifies the passive components requiring correction.

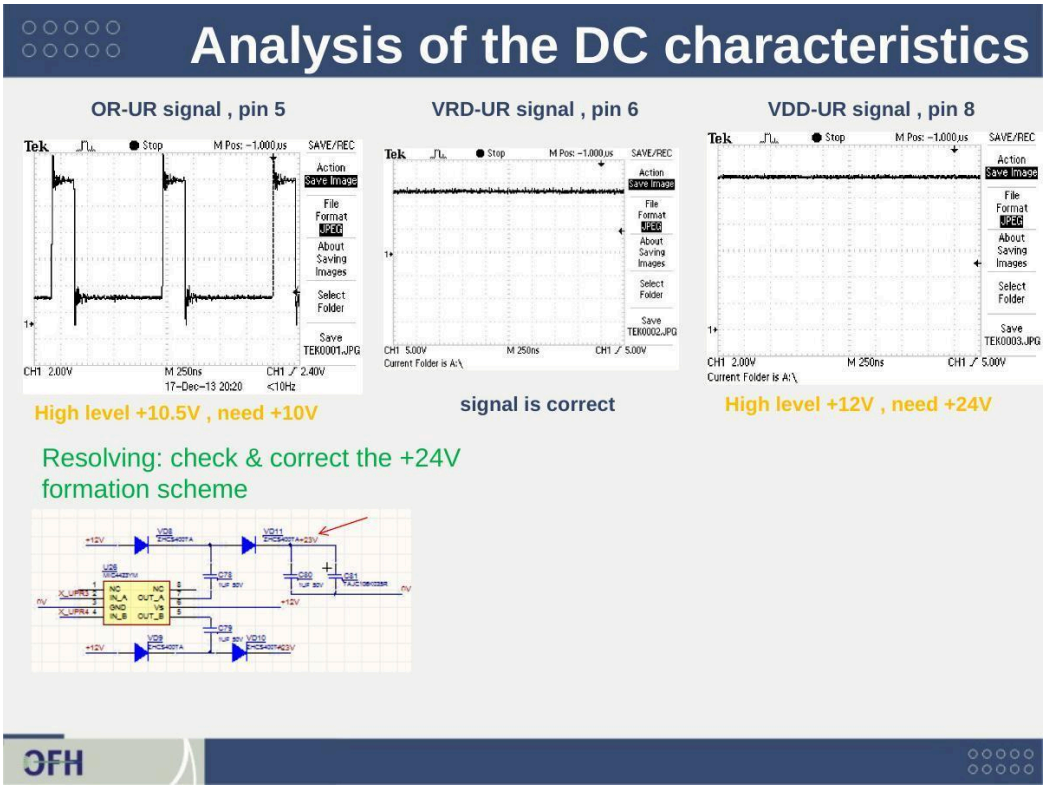


Figure 5: Oscilloscope measurements of OR-UR (pin 5), VRD-UR (pin 6), and VDD-UR (pin 8). VDD-UR measured +12V (required +24V) — a 50% deficit in the supply voltage. OR-UR measured +10.5V vs. required +10V (marginal). VRD-UR was correct. The +24V generation schematic (bottom) shows the charge-pump circuit requiring passive component corrections.

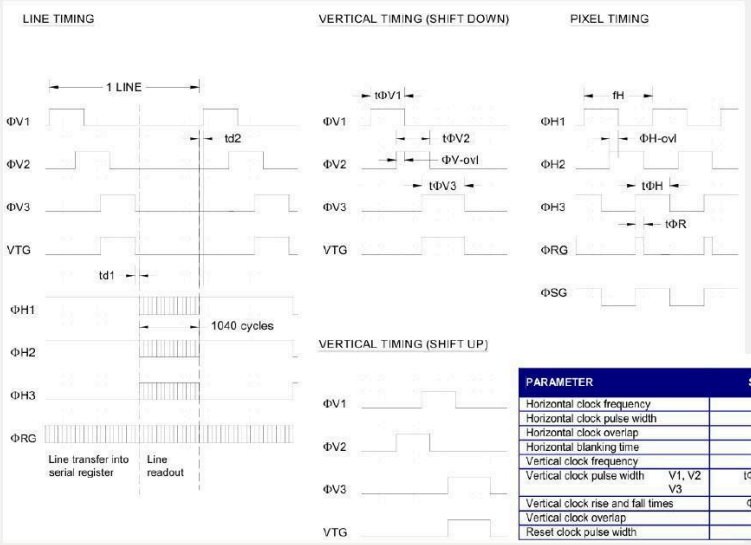
- V1, V2, V3 vertical clock signals (pins 2, 3, 4 and 20, 21): high level measured at +5V, required +2.5V
- VRD-UR (pin 6): high level measured at +12V, required +24V
- H1, H3 horizontal clock signals: low level measured at −6V, required −5V
- All out-of-spec levels traced to incorrect passive component values in the level-shifting circuits — resistor and capacitor value corrections identified for each affected channel

5.5 CCD Clock Timing Analysis

Oscilloscope measurement of the CCD clock timing waveforms was performed and compared against the Perkin Elmer datasheet timing diagrams covering line timing, vertical timing (shift down and shift up), and pixel timing. The vertical clock overlap time (V-ovl, the period during which ΦV1 and ΦV2 are both high during a vertical shift) was measured at 0 µs — the datasheet specifies 26 µs as the typical value. All other timing parameters were within specification.

Analysis of the CCD interface clock timing

Description of tasks: verifying the signals on CCD with an oscilloscope, comparison the clock timing characteristics with the documentation



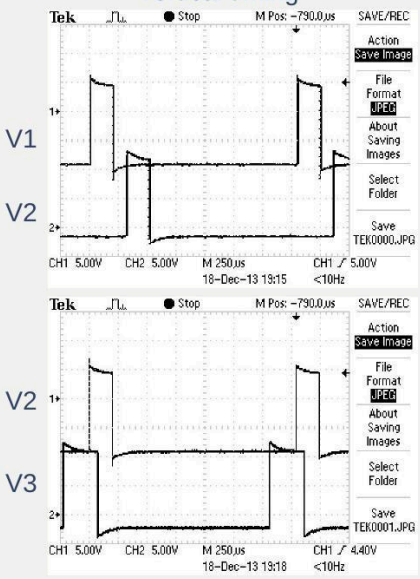
TYPICAL CLOCK TIMING

PARAMETER		SYMBOL	VALUE	UNIT
Horizontal clock frequency		f_H	400	kHz
Horizontal clock pulse width		tΦH	1.25	µs
Horizontal clock overlap		f_H-ovl	0.3	µs
Horizontal blanking time		H-blank	600	µs
Vertical clock frequency		f_V	2.5	kHz
Vertical clock pulse width	V1, V2	tΦV1, tΦV2	200	µs
	V3	tΦV3	300	µs
Vertical clock rise and fall times		ΦVtr, ΦVtf	200	ns
Vertical clock overlap		f_V-ovl	26	µs
Reset clock pulse width		tΦR	300	ns

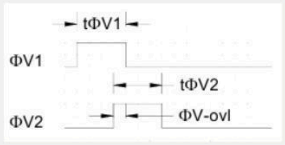
Figure 6: CCD interface clock timing diagram from the Perkin Elmer datasheet, covering line timing (ΦV1–ΦV3, VTG, ΦH1–ΦH3), vertical timing (shift down and shift up sequences), and pixel timing. The typical clock timing table specifies the key parameters: horizontal clock frequency 400 kHz, vertical clock overlap f_V-ovl = 26 µs, reset clock pulse width tΦR = 300 ns.

Analysis of the CCD interface clock timing

Vertical timing

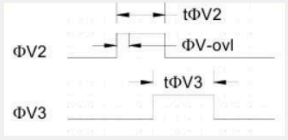


Vertical timing(documentation)



V-ovl = 0us need 26us

tV1, tV2 is correct



V2 need before V3

Resolving: need to correct timing on FPGA

Figure 7: Oscilloscope measurement of CCD vertical clock timing showing the V-ovl defect. Top traces: measured V1/V2 waveforms — V2 transitions to high before V1 goes low, giving V-ovl = 0 µs. Right: datasheet timing diagram showing the required 26 µs V-ovl overlap period where both ΦV1 and ΦV2 are simultaneously high. Resolution: FPGA firmware timing parameter correction.

5.6 Analog Front-End Analysis

Analysis of the pre-amplifier circuit with no input signal (black level measurement) revealed a systematic offset difference between the two CCD output channels — channel 1 and channel 2 black levels were not equal. This offset would manifest as a brightness difference between the two halves of the image when the channels are interleaved. Resolution: the FPGA firmware was updated to measure and store the individual black-level offset for each channel at startup and subtract it digitally during image reconstruction — a calibration approach that eliminates the brightness artifact without requiring analog component changes.

5.7 Host Application Software

OFH delivered a complete Windows host application (C#/.NET Framework 4) providing a graphical interface for the spectrometer system. This software was a deliverable alongside the firmware and hardware corrections — enabling the client to operate the instrument without writing their own PC-side integration code. Key features:

- Dual communication interfaces: USB (automatic initialization and device detection with error diagnostics) and RS-232 (selectable COM port, auto baud rate detection with status confirmation)
- CCD acquisition control: pixel readout frequency selection, integration time (exposure) in milliseconds, frames addition with optional averaging (1–32 frames), operation mode (cyclic or single capture), and external trigger synchronization
- Binning control: variable binning from 1× (full 2048×2048) to 1024× (2048×2 pixels), supporting both full-resolution and signal-averaging configurations
- Temperature monitoring: onboard ADC temperature, dual CCD thermistor readout (CCD1 and CCD2), and TEC PWM duty cycle control (0.0000–1.0000, resolution <0.0001)
- Image display and analysis: real-time image viewer with contrast stretch, fit-to-window scaling, pixel coordinate and 16-bit intensity readout, and histogram analysis of user-selected regions with standard deviation and average statistics

6. Technical Significance

This multi-phase engagement demonstrates OFH's capability to provide sustained electronics engineering support across the full lifecycle of a photonics instrument — from new board design through production bring-up and field debug. Key technical contributions across the three phases:

- Complete host application software (C#/.NET): a full Windows GUI enabling CCD acquisition control, TEC management, USB/RS-232 communication, real-time image display with histogram analysis, and

16-bit data export — delivered alongside the hardware and firmware, providing the client with a turnkey instrument operation environment.

- FPGA/NIOS system architecture for a high-speed spectrometer controller: coordinating resonant scanner phase decoding, multichannel ADC acquisition at 1000 points per 1.3 ms, and USB 2.0 high-speed data transfer to the host PC.
- Custom SMD PCB design with complete US-sourced BOM: Altera Cyclone III FPGA, FTDI USB FIFO, 16-bit ADCs, precision voltage references, and multi-rail power management in a compact (<60×96 mm) RoHS-compliant board.
- Mixed-signal board design discipline: separate analog and digital ground planes joined at a single point, precision reference supply routing, and ADC placement for optimal signal quality — all identified as necessary corrections during the Phase 3 analysis, confirming the importance of these practices in the Phase 2 design.
- Systematic USB interface debug methodology: test program development, oscilloscope-based signal characterization, and root-cause identification of both hardware (bus current, line noise) and software (reconnection logic) failure modes.
- CCD interface analysis: quantitative comparison of all drive voltage levels and timing parameters against datasheet specifications, with specific passive component corrections identified for each out-of-spec signal — enabling targeted rework rather than board redesign.

7. About Optics for Hire

Optics for Hire (OFH) is an optical engineering consultancy based in Arlington, Massachusetts. Since 2002, OFH has delivered optical and photonics engineering services to clients ranging from startups to Fortune 50 corporations. Our R&D team of 12 engineers includes physicists, optics PhDs, and electronics and software engineers — enabling us to address the full system stack from optics through electronics to firmware and software.

OFH electronics and embedded systems capabilities include:

- FPGA design (Altera/Intel, Xilinx) including embedded soft-processor (NIOS II, MicroBlaze) development
- Custom SMD PCB design in Altium Designer — analog, digital, and mixed-signal boards
- High-speed ADC/DAC interface design for photodetector and CCD readout
- USB 2.0 and RS-232 interface implementation
- CCD and photodetector front-end electronics (PbS, InGaAs, silicon PIN, APD)
- Power management for precision analog/digital mixed-signal boards
- Board bring-up, debug, and systematic signal integrity analysis
- Complete BOM generation with US distributor sourcing

Electronics & Firmware	Imaging Optics	Illumination Design	System Integration
FPGA, embedded processors, ADC/DAC, USB, CCD/detector readout, PCB design	Flow cytometry, NIR imaging, surgical cameras, machine vision, objectives	TIR lenses, reflectors, Fresnel lenses, grow lights, architectural luminaires	Spectrometer systems, medical devices, optical data storage, industrial instruments

8. Contact

To discuss a custom electronics design, FPGA development, or photonics instrument electronics project — contact us:

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Electronics Capabilities

→ FPGA design (Altera Cyclone, Xilinx) + NIOS II / soft-processor
→ Custom SMD PCB design — Altium Designer
→ High-speed ADC/DAC interface for detector readout
→ USB 2.0 HS and RS-232 implementation
→ CCD and photodetector front-end electronics
→ Mixed-signal power management design
→ Board bring-up, systematic signal integrity debug
→ US-sourced BOM generation (Digi-Key, Mouser, Newark)
→ Spectrometer and photonics instrument control electronics